LESSON PLAN

SUB: DIGITAL ELECTRONICS & COMPUTER ORGANISATION
BRANCH:- COMPUTER SCIENCE& ENGG.
SEMESTER:3rd
NAME OF FACULTY: LAXMIDHAR SETHY (Sr. Lect . in CSE)

GOVERNMENT POLYTECHNIC, BHADRAK

SESSION: 2025-26

Hod ,CSE

Academic Co-ordinator

Academic Co-ordinator

Principal

Govt. Polytechnic, Bhadrak

DEPARTMENT OF Computer Science & Engg.,

Discipline: Computer Sc. & Engg.	Semester:3rd	Name of the Faculty: Sri Laxmidhar Sethy Email ID-ldsathy@gmail.com
Subject: Digital Electronics & Computer Organisation	No. Of Days/Week Class Allotted- 3	Semester From Date: 01.07.2026-05.11.2027 No. of Weeks:
Week	Class Day	Theory Topics
1st	1st	Introduction to Digital Electronics
	2nd	Difference Between Analog and Digital Signals
	3rd	Number Systems: Binary, Octal, Decimal, and Hexadecimal Conversion Between Number Systems,
2nd	1st	Number Systems: Binary, Octal, Decimal, and Hexadecimal Conversion Between Number Systems, Binary Arithmetic Boolean Algebra
	2nd	Binary Arithmetic Boolean Algebra Basic Operations, Laws, and Simplification
	3rd	Binary Arithmetic Boolean Algebra
3rd	1st	Basic Operations, Laws, and Simplification
	2nd	Logic Gates and Circuit, Logic Gates: AND, OR, NOT, NAND, NOR, XOR, XNOR
	3rd	Logic Gates: AND, OR, NOT, NAND, NOR, XOR, XNOR
4th	1st	Design and Simplification of Logic Circuits Using Boolean Algebra
	2nd	Design and Simplification of Logic Circuits Using Boolean Algebra
	3rd	Karnaugh Maps (K-Maps) for Simplification Practical Applications of Logic Gates in Real-World Circuits
5th	1st	Karnaugh Maps (K-Maps) for Simplification Practical Applications of Logic Gates in Real-World Circuits
	2nd	Combinational circuits : multiplexers and demultiplexers , encoders and decoders
	3rd	Sequentional circuits : flip-flops (SR, JK, D, T) and their applications
6th	1st	Sequentional circuits : flip-flops (SR, JK, D, T) and their applications
	2nd	Counters : synchronous and asynchronous counters
	3rd	Registers and Shift Registers: Types and Uses
7th	1st	Instruction Cycle: Fetch, Decode, Execute
	2nd	Instruction Cycle: Fetch, Decode, Execute

	3rd	Memory Organization: Types of Memory (RAM, ROM, Cache, Virtual Memory)
8th	1st	Memory Organization: Types of Memory (RAM, ROM, Cache, Virtual Memory)
	2nd	Introduction to Buses: Address Bus, Data Bus, and Control Bus
	3rd	Introduction to Buses: Address Bus, Data Bus, and Control Bus
9th	1st	Processer architecture and control unit
	2nd	Unit introduction to microprocessors and microcontrollers
	3rd	Basics of arithmetic logic unit & contol unit
10th	1st	Instruction set architecture
	2nd	RISC vs CISC
	3rd	Pipelining and performance optimization in processors
11th	1st	Pipelining and performance optimization in processors
	2nd	Input output systems and i/o devices
	3rd	i/o devices and interfaces: keyboard , mouse, printers
12th	1st	i/o devices and interfaces: keyboard , mouse, printers
	2nd	Storage devices interrupts and DMA(direct memory access)
	3rd	Overview of modern trends :Multicore processors , GPUs, Embedded systems
13th	1st	Mini project : design a simple digital circuit or simulate a basic CPU operation
	2nd	Mini project : design a simple digital circuit or simulate a basic CPU operation
	3rd	Questions answer discussion
14th	1st	Questions answer discussion
	2nd	Revision
	3rd	Revision
15th	1st	**Quiz test**
	2nd	**Possible questions discussion**
	3rd	**Possible questions discussion**

Signature of Faculty