LESSON PLAN

SUB: DIGITAL ELECTRONICS LAB
BRANCH:- COMPUTER SCIENCE& ENGG.
SEMESTER:3RD
NAME OF FACULTY: LAXMIDHAR SETHY(Sr. Lecturer in CSE)

GOVERNMENT POLYTECHNIC, BHADRAK

SESSION: 2025-26

Hod ,CSE

Academic Co-ordinator

Academic Co-ordinator

Principal
Govt. Polytechnic, Bhadrak

DEPARTMENT OF Computer Science & Engg.,

LESSON PLAN

Discipline: Computer Sc. & Engg.	Semester:3rd Winter-2025	Name of the Faculty: LAXMIDHAR SETHY
Subject: DIGITAL ELECTRONICS LAB	No. Of Days/Week Class Allotted- 4	SemesterFromDate:14/07/2025 ToDate:15/11/2025 No. of Weeks:15
Week	**Class Day**	**Theory Topics**
1st	1ST	To verify the truth tables for all logic gates: NOT, OR, AND, NAND, NOR, XOR, XNOR using CMOS Logic gates and TTL Logic Gates.
	2ND	To verify the truth tables for all logic gates: NOT, OR, AND, NAND, NOR, XOR, XNOR using CMOS Logic gates and TTL Logic Gates.
2nd	1ST	To verify the truth tables for all logic gates: NOT, OR, AND, NAND, NOR, XOR, XNOR using CMOS Logic gates and TTL Logic Gates.
	2ND	Implement and realize Boolean Expressions with Logic Gates
3rd	1ST	Implement and realize Boolean Expressions with Logic Gates
	2ND	Implement and realize Boolean Expressions with Logic Gates
4th	1ST	Implement Half Adder, Full Adder, Half Subtractor, Full Subtractor using ICs
	2ND	Implement Half Adder, Full Adder, Half Subtractor, Full Subtractor using ICs
5th	1ST	Implement Half Adder, Full Adder, Half Subtractor, Full Subtractor using ICs
	2ND	Implement parallel and serial full-adder using ICs.
6th	1ST	Implement parallel and serial full-adder using ICs. Implement parallel and serial full-adder using ICs.
	2ND	Design and development of multiplexer and De-multiplexer using multiplexer ICs

7th	1ST	Design and development of multiplexer and De-multiplexer using multiplexer ICs
	2ND	Design and development of multiplexer and De-multiplexer using multiplexer ICs
8th	1ST	Verification of the function of SR, D, JK, and T Flip Flops.
	2ND	Verification of the function of SR, D, JK, and T Flip Flops.
9th	1ST	Verification of the function of SR, D, JK, and T Flip Flops.
	2ND	Verification of the function of SR, D, JK, and T Flip Flops.
10th	1ST	Design controlled shift registers.
	2ND	Design controlled shift registers.
11th	1ST	Design controlled shift registers.
	2ND	Construct a Single Digit Decade Counter (0-9) with a 7-segment display.
12th	1ST	Construct a Single Digit Decade Counter (0-9) with a 7-segment display.
	2ND	Construct a Single Digit Decade Counter (0-9) with a 7-segment display.
13th	1ST	Construct a Single Digit Decade Counter (0-9) with a 7-segment display.
	2ND	To design a programmable Up-Down Counter with a 7-segment display.
14th	1ST	To design a programmable Up-Down Counter with a 7-segment display.
	2ND	To design a programmable Up-Down Counter with a 7-segment display.
15th	1ST	To design a programmable Up-Down Counter with a 7-segment display.
	2ND	Previous Year Question and Answer

Signature of Faculty